Initial Test Steps for BNL711 V1P5 Cards

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Contents

1 Tests to do when get a new card

1.1 Power

- Check whether the 10 DC-DC outputs are right.
- Assemble the sensor resistors; enable the sensing function for MGTAVTT, MGTAVCC, and VCCINT.
- Assemble resistors to enable 0.6 V power for DDR4, and power for ORx (TTC optical module).
- Assemble the ORx.

1.2 FPGA

The JTAG can find the FPGA. The Flash can be written via JTAG.

1.3 Transceivers

Connect all of the 48 optical fibre links as loopback (or from one card to another). Program the FPGA with the 12.8 Gb/s IBERT bit file.

- Run with PRBS31 for a long time until the BER is smaller than 1E-15. Sometimes the QPLL must be reset to bring up the links.
- Also the 9.6 Cb/s with QPLL/CPLL can be tested, which will be used by the FULL mode of FELIX.
- This test results shows that (for PRBS testing):
  - CPLL 9.6G: when set the RXTERMMODE to be ”floating”, it is better than ”programmable” (though programming is suggested for with external AC coupling), the open area can increase 500-800. If RXLPMEN=1, the open area increases: for the card with the worst performance, it changes from 3960 to 7037.
  - QPLL 12.8G: RXLPMEN=1 increase the open area. for the card with the worst performance, it changes from 4236 (about 300-700 smaller than other cards) to 5821 .
  - We need more test to check how to set the above equalization mode and termination. Current suggestion is to set termination as AC, programming, 800mV (default setting by the wizard); and use LPM mode for equalization.
- Please make sure the fiber connection is OK, especially the connection with MiniPODs.

The LMK03200 is used for the link speed testing.

1.4 DDR4

DDR4 can use several system clocks.

- CLK1: internal MMCM generates DDR4 system clock, and send to dedicated clock pins via external traces.
- CLK2: internal MMCM generates DDR4 system clock, and directly connect to DDR4 firmware module. DRC errors occur, it can be disabled by *tcl* command.
- CLK3: use SI5345 to generate reference clock.
- CLK4: FPGA receiver external reference clock via SMP connectors, and send to dedicated clock pins via external traces.
- Basically, CLK3 & CLK4 are better than CLK2, CLK1 is the worst.
- For the V1.5 PCB, DDRA performance is better than DDRB. DDRA always works well for 2.11 GT/s with CLK1; for DDRB, some cards have issue when using CLK1 (or even with CLK2) for 2.11 GT/s, but all clocks work for 2.00 GT/s.

1.5 TTC Circuit

Connect the TTC signal (data and clock) to two SMP connectors, verify it with scope.

1.6 System Integration

Integration test with FELIX firmware example.

1.6.1 PCIe Endpoints

sudo lspci -vvv can get see $\times$8 lane Xlinx PCIe endpoints.

1.6.2 SI5345 Configuration

To configure it with FELIX software. See the other document.

1.6.3 Flash Writing Via PCIe

Firmware receives bit file from PCIe, and update the Flash partition. FELIX firmware and software already support FLASH R/W.

1.7 Micro-controller

- Program the Micro-controller via the AVR-Dragon programmer.
- Use i2ctools to set the I2C switch on-board, to connect the SMBus to the micro-controller.
- Use i2ctools to communicate with uC, and program the FPGA from different bit files.

1.8 Channel Mapping

See the slides.

with current mapping as in the slides, we can use a 48 lines fiber to connect the two MTP couplers, to test all the 48 channels. The sequence of the 4 ribbons in the upper MTP coupler can also be swapped, to make the two MTP fibers have same sequence for TX & RX.